Silicon Labs Introduces the Industry's Lowest Jitter Clock Generator for Broadcast Video Applications

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AUSTIN, Texas, Sep 14, 2009 (BUSINESS WIRE) -- Silicon Laboratories Inc. (NASDAQ: SLAB), a leader in high-performance, analog-intensive, mixed-signal ICs, today introduced the expansion of its Any-Rate Precision Clock family with the Si5324, the industry's lowest jitter, most highly integrated clock IC optimized for professional broadcast video applications. The Si5324 replaces traditional multi-component video PLL solutions with a single clock IC while providing 80 percent lower jitter than competing solutions. The Si5324 can generate virtually any output frequency from 2 kHz to 1.4 GHz from any input frequency ranging from 2 kHz to 710 MHz, simplifying synchronization in next generation multi-rate video equipment. This makes the Si5324 ideal for video capture, conversion, editing, display, and distribution equipment that must be synchronized within video studios.

Clock generation and synchronization are becoming increasingly complex in broadcast video applications. The process, known as genlock, of synchronizing all video equipment to a common sync source has become challenging due to the proliferation in the number of HD video formats and frame rates that must be supported. Additionally, the industry's migration to high-speed 3G-SDI requires improved jitter performance in comparison to legacy video standards, increasing the design challenge for equipment makers. Traditional genlock solutions require discrete VCXO and filter components, support a limited range of input/output frequencies and suffer from relatively poor jitter performance in comparison to 3G-SDI requirements.

The industry's lowest jitter clock generator for genlock applications, the Si5324, addresses these challenges, delivering jitter performance of 5 ps pk-pk, providing significant margin to all existing and emerging video standards including 3G-SDI (SMPTE 424M). By meeting these standards with considerable margin, the jitter budget that would otherwise be allocated to clock generation can be applied to other components in the system, simplifying component selection and design.

The Si5324 incorporates all PLL components into a single highly integrated device, eliminating the need for multiple PLL ICs, external filters and VCXO components. Based on Silicon Labs' patented DSPLL(R) technology, the Si5324 has a fully integrated, digitally programmable loop filter that supports loop bandwidths ranging from 4 to 525 Hz as well as a low phase noise internal VCO. The DSPLL(R) technology enables the Si5324 to provide jitter filtering while also eliminating sensitive noise entry points between loop filter and VCXO components, reducing design complexity and simplifying layout. Any-rate capability makes it possible for the Si5324 to generate and synchronize all common HD video and audio reference frequencies without any component changes, allowing one design for multiple applications and simplifying design re-use.

"Silicon Labs patented DSPLL technology is what enables the Si5324 to dramatically simplify the discretely implemented timing architectures used in broadcast video systems," said Dave Bresemann, vice president of Silicon Laboratories. "By consuming less than a tenth of the overall 3G-SDI jitter budget and offering any-rate frequency flexibility, the Si5324 helps customers achieve first pass success and enables a single IC design for multi-frequency applications, a significant time, system cost and resource savings."

Complementing the Si5324, Silicon Labs offers crystal oscillators (XOs) and voltage-controlled crystal oscillators (VCXOs) ideally suited for broadcast video applications. Silicon Labs' Si590/591/595 family of XO/VCXOs provides cost-effective low jitter clock generation and supports any frequency from 10 to 525 MHz, any format (CMOS, LVDS, LVPECL, CML) and any supply voltage (1.8, 2.5, or 3.3 V), with guaranteed low jitter of 1 ps rms (max). The Si59x family is the newest addition to Silicon Labs' portfolio of oscillators that includes single, dual, quad, and any-rate I2C programmable XO/VCXOs, devices that can dramatically simplify clock generation and reduce BOM cost in multi-rate HD SDI applications. Any frequency/format /VDD/stability XO/VCXO is available from Silicon Labs with 2 week lead times without NRE or minimum order quantity (MOQ) restrictions.

Pricing and Availability

The Si5324 is packaged in a space-saving 36-lead, 6x6 mm QFN package with samples and production quantities available now. The Si5324 is priced at $17.95 to $57.20 depending on the selected output clock frequency range (A/B/C/D speed grades) in 1k quantities. The Si590/591/595 XO/VCXOs are available now in an industry standard 5x7 mm package. The Si590/591 XOs are priced between $4.08 and $8.50 in 10k quantities depending on frequency and stability. The Si595 VCXO is priced between $4.89 and $11.48 in 10k quantities depending on frequency and stability. Please visit our website to buy, sample or build a part number.

Silicon Laboratories Inc.

Silicon Laboratories is an industry leader in the innovation of high-performance, analog-intensive, mixed-signal ICs. Developed by a world-class engineering team with unsurpassed expertise in mixed-signal design, Silicon Labs' diverse portfolio of highly integrated, easy-to-use products offers customers significant advantages in performance, size and power consumption. These patented solutions serve a broad set of markets and applications including consumer, communications, computing, industrial and automotive.

Headquartered in Austin, TX, Silicon Labs is a global enterprise with operations, sales and design activities worldwide. The company is committed to contributing to our customers' success by recruiting the highest quality talent to create industry-changing innovations. For more information about Silicon Labs, please visit www.silabs.com.

Cautionary Language

This press release may contain forward-looking statements based on Silicon Laboratories' current expectations. These forward-looking statements involve risks and uncertainties. A number of important factors could cause actual results to differ materially from those in the forward-looking statements. For a discussion of factors that could impact Silicon Laboratories' financial results and cause actual results to differ materially from those in the forward-looking statements, please refer to Silicon Laboratories' filings with the SEC. Silicon Laboratories disclaims any intention or obligation to update or revise any forward-looking statements, whether as a result of new information, future events or otherwise.

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