



Silicon Laboratories Introduces Industry's First Jitter Attenuating 10 Gbps XFP Transceiver IC; Si5040 Offers Small Size, Low Jitter and Low Power for XFP Optical Module Applications

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Achieving best-in-class jitter performance, the Si5040 uses Silicon Laboratories' patented DSPLL technology to reduce jitter on 10 Gbps serial data streams that have been degraded by system level noise sources on either the network side or the port card. This revolutionary new transceiver architecture provides industry-leading transmit jitter generation of 2.5 mUI RMS while eliminating the need for external jitter clean up circuitry inside the module or on the port card. Applying DSPLL technology in the receive path minimizes receive data jitter to ensure error-free operation with port card ASICs or FPGAs.

The Si5040 uses an innovative receiver circuit that automatically adjusts data recovery parameters to optimize bit-error-rate (BER) performance ensuring robust operation in unpredictable multi-vendor network environments over a wide range of channel conditions. Receiver performance is optimized by using an internal signal quality monitor to drive real-time adjustment of the decision threshold so that BER performance and jitter tolerance is maximized. The Si5040 also supports manual adjustment of the receiver decision threshold and sampling phase for custom BER optimization algorithms. Regardless of receiver operating mode, the superior input sensitivity (5 mV pk-pk differential typical) of the Si5040 makes it ideal for both short and long reach applications.

"The Si5040 continues to deliver on Silicon Laboratories' commitment to providing innovative solutions to the networking industry by leveraging our industry leading DSPLL technology," said Dave Bresemann, vice president of Silicon Laboratories. "By combining jitter attenuation capability together with a sophisticated receiver architecture, we are greatly simplifying the task of achieving true SONET/SDH performance in XFP module applications."

The Si5040 XFP transceiver offers the industry's most complete feature set including support for three types of analog and digital signal quality monitors including analog loss-of-signal (LOS) detection, consecutive identical digit (CID) detection and a proprietary digital measure of receive data eye opening. The Si5040 also simplifies system level test and debug by offering line loop-back, XFI loop-back and PRBS pattern generation and checking on both transmit and receive data paths. Complete device configuration and status monitoring is available through a serial microcontroller interface supporting commonly used protocols such as I2C.

To support the industry's need for low power solutions, the Si5040 consumes less than 575 mW typical. The Si5040 further simplifies power management by operating over a wide power supply variation from +5% to -10% and provides additional power savings through programmable signal swings on all high-speed outputs. By operating over the full industrial temperature range (-40 degrees C to +85 degrees C), the Si5040 accommodates demanding module thermal conditions.

Pricing and Availability

The Si5040 is available in a 5 x 5 mm, lead-free, RoHS-compliant, 32-pin quad flat no-lead (QFN) package. Samples are available now with production scheduled for the second quarter of 2006. Pricing for the Si5040 is \$38.25 in quantities of 1k.

Silicon Laboratories Inc.

Silicon Laboratories Inc. is a leading designer of high-performance, analog-intensive, mixed-signal integrated circuits (ICs) for a broad range of applications. Silicon Laboratories' diverse portfolio of highly-integrated, patented solutions is developed by a world-class engineering team with decades of cumulative expertise in cutting-edge mixed-signal design. The company has design, engineering, marketing, sales and applications offices throughout North America, Europe and Asia. For more information about Silicon Laboratories, please visit www.silabs.com.

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